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Design and Implementation of Bpsk Modulator and Demodulator Using Vhdl

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Abstract: *This paper give the brief description of digital communication system.Digital communication is more reliable, secure and efficient than that of analog communication.In Digital communication,BPSK is most important and efficient technique in terms of signal power. In this paper BPSK modulator and demodulator are purely design by using hardware description language (VHDL) and implementing it on Spartan 3E FPGA kit.*

I. Introduction

In the last years, a major transition from analog to digital modulation techniques has occurred and it can be seen in all areas of wireless communication, satellite and cellular systems.

A digital communication system is more reliable than an analog. The aim of the paper is to create a BPSK (Binary Phase Shift Keying) modulator and demodulator using Xilinx ISE 12.3 software. BPSK consist of modulator a channel and demodulator. The modulated signal was achieved in the first Spartan 3E board, passed through a channel and transmitted to the second board, which behaves as a demodulator.

II. Theoretical Backgrounds

A. Digital Communication System:

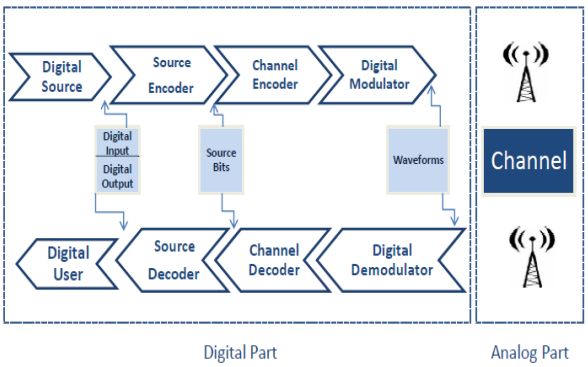

Figure 1. A Digital Communication System

The typical block diagram of digital communication system is presented in Fig.1.The digital communication system consist of both digital and analog parts. The digital part consists of digital source/user, source encoder/ decoder, channel encoder/decoder and the digital modulator or demodulator. The analog part is made of the transmitter, receiver, the channel models and noise models.

The message to be sent is from a digital source, in our case, from a computer. The source encoder accepts the digital data and prepares the source messages. The role of the channel encoder is to map the input symbol sequence into an output symbol sequence. The binary information obtained at the output of the channel encoder is than passed to a digital modulator which serves as interface with the communication channel. The main purpose of the modulator is to translate the discrete symbols into an analog waveform that can be transmitted over the channel. In the receiver, the reverse signal processing happens. A channel is the physical medium that carries a signal between the transmitter and the receiver. The signal is corrupted with noise whatever the medium used for transmission.

In the receiver, the reverse signal processing happens. A channel is the physical medium that carries a signal between the transmitter and the receiver. The signal is corrupted with noise whatever the medium used for transmission. The role of a digital communication system is to transport digital data between the transmitter and receiver. As the signals propagate between the two nodes, they may be submitted to distortion due the channel imperfection. The digital data is transmitted between the transmitter and the receiver by varying a physical characteristic of a sinusoidal carrier, either the frequency or the phase or the amplitude. This operation is performed with a modulator at the transmitting end to impose the physical change to the carrier and a demodulator at the receiving end to detect the resultant modulation on reception.

B.Basic BPSK Modulator and Demodulator:

Digital modulation is the process by which digital symbols are transmitted into waveforms that are compatible with the characteristics of the channel. The modulation process converts the signal in order to be compatible with available transmission facilities. At the receiver end, demodulation must be accomplished by recognizing the signals. The modulation technique used in this project is BPSK (Binary Phase Shift Keying) and it is widely used in digital transmission.. BPSK modulation is the simplest form and most robust of all the PSK modulation techniques. The BPSK modulator is quite simple and is illustrated in fig.2. The binary sequence m(t) or modulating signal is multiplied with a sinusoidal carrier and the BPSK modulated signal s(t) is obtained. The output of the BPSK signal generated by the modulator is shown in Fig 3.

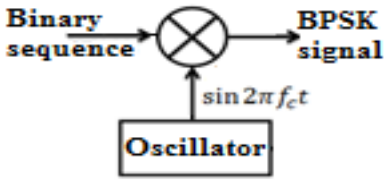

Figure 2. BPSK Modulator

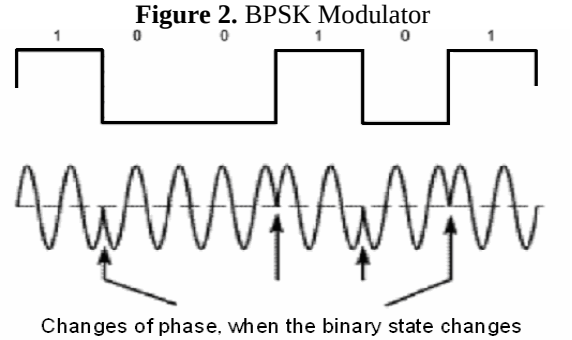

Figure 3. BPSK Modulator output

At the receiver side to demodulate the signal, it is necessary to reconstitute the carrier. This process is made in the Carrier Recovery Circuit. Next, the BPSK modulated signal is multiplied with the carrier, pass through an integrator and then decision circuit will give the modulating signal at the end.

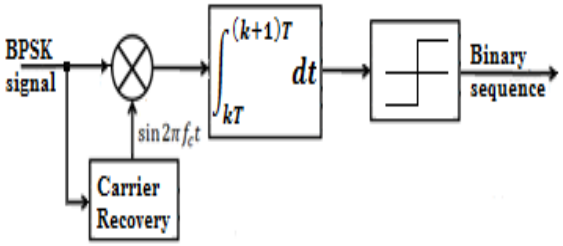

Figure 4. BPSK Demodulator

III. Design of BPSK Modulator:

Block diagram of BPSK modulator is shown in figure 5. It consists of DDS Compiler, LFSR, and a mux. The modulating signal which are in the form of binary digits i.e. 0 and 1, are generated internally by a LFSR (Linear Feedback Shift Register). DDS Compiler Block is a direct digital synthesizer which is the main part of the system which is use to generates the carrier i.e sinusoids.DDS uses a lookup table scheme to generate sinusoids. A digital integrator generates a phase that is mapped by the lookup table into the output waveform. The mux block implements a multiplexer. It has one select input and a configurable number of data inputs that can be defined by the user. The d0 and d1 inputs of mux represent the sine waves. The sel input of mux represents the modulating signal and selects between the d0 and d1 inputs. If LFSR is '1', the modulated signal remained same as the carrier, but if '0' was transmitted, then the carrier is shifted by 180º phase shift. At the output we will get the modulated signal. The expected waveforms at the modulator side are shown in figure 6. Results of modulator and its different blocks are shown in fig 10.

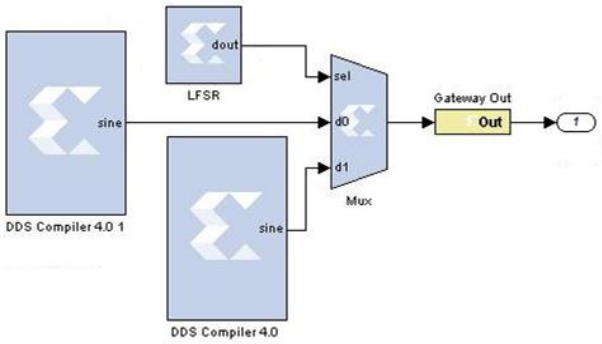

Figure 5. BPSK Modulator

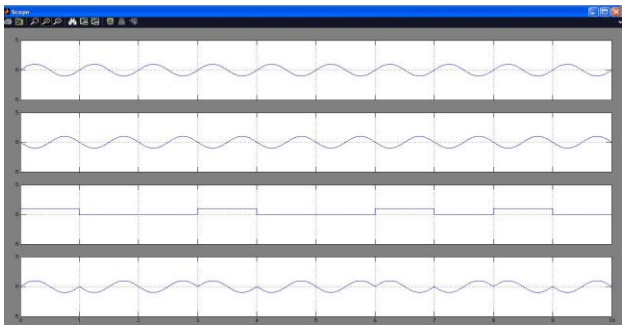

Figure 6.(1)carrier signal(2) 180º phase shift carrier(3) modulating signal(4) modulated signal

IV. Design of BPSK Demodulator

Block diagram of BPSK demodulator is shown in figure 7.The modulated signal which was transmitted by modulator is then pass through the channel and received at the input of demodulator. The carrier is recovered due to the DDS compiler and then multiplied with the modulated signal affected by noise. The obtained signal is then added with all the samples, multiplied, from a period. This operation takes place in the accumulator. Once we have a result, it is compared with a threshold.

If the compared signal is positive, the demodulator takes the decision that '1' was transmitted, otherwise, '0' is the result. Figure 8 illustrates the expected modulating signal generated in the modulator and the demodulated signal obtained after the demodulation operation.

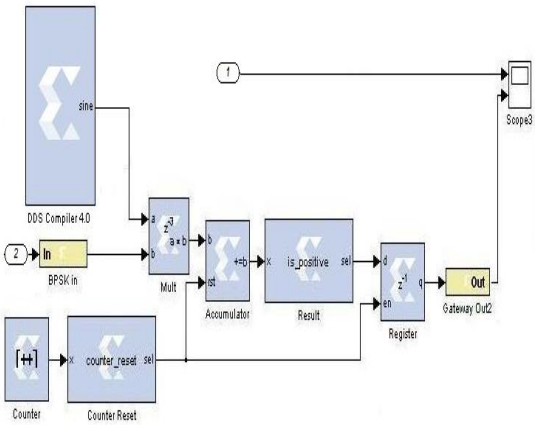

Figure 7. BPSK Demodulator

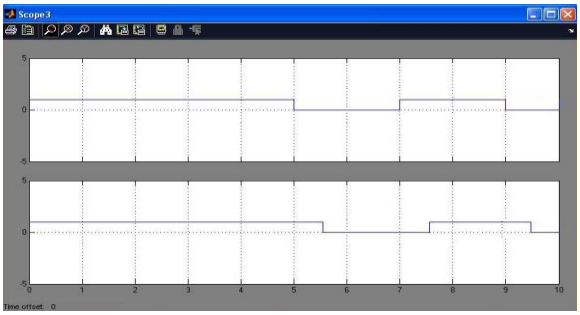

Figure 8. (a) The modulating signal (b) The demodulated signal

V. Design of BPSK System On The SPARTAN 3E Board

The BPSK system on FPGA kit is shown in figure 9. It consists of two Spartan 3E boards, first behaves as a modulator and the second one, as a demodulator. The connections between the two boards are made of three wires: first comports as a communication channel, the second as an asynchronous reset signal and the last one for the synchronization of the two boards.

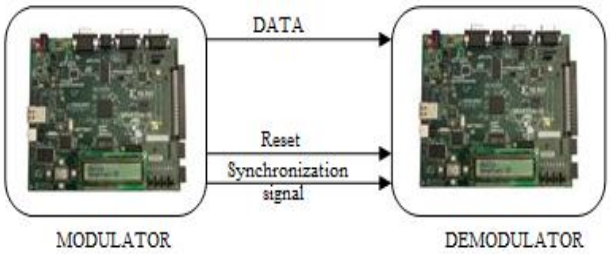

Figure 9 .BPSK System.

VI. Results

1)Modulator part:

Fig 10(a) represent the linear feedback shift register which is use to generate the input data.fig 10(b) illustrate the output waveform and 8bit sequence of LFSR.

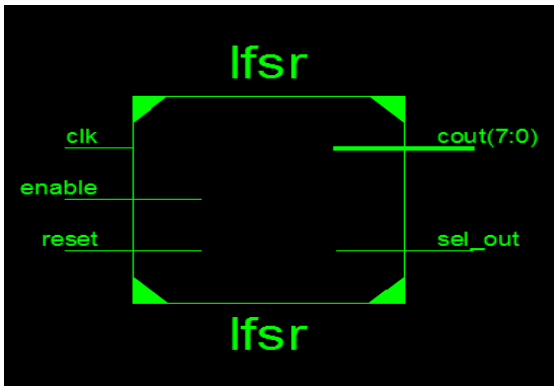

Fig 10 (a). LFSR RTL view

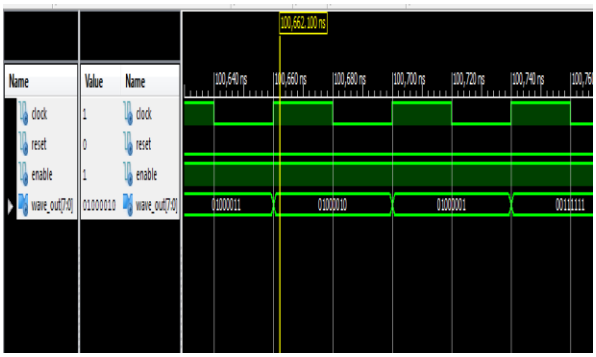

Fig 10 (b). LFSR Output waveform

Fig 10(c) represent the carrier generation block which is use to generate the sinusoidal waveform..fig 10 (d) illustrate the sinusoidal waveform.

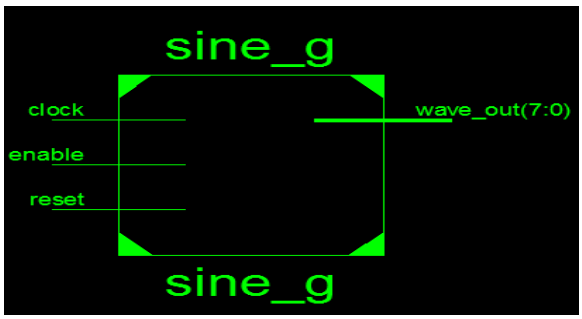

Fig 10 (c). RTL view of DDS Compiler

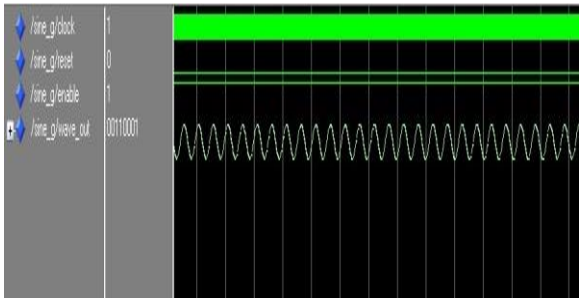

Fig 10 (d). DDS Compiler output waveform

Fig 10(e) shows the complete modulator block. The output waveform of modulator in Xilinx is shown in fig 10 (f).Fig 10(g) shows the modulator output using
Modelsim software to clearly see the sinusoidal waveforms.

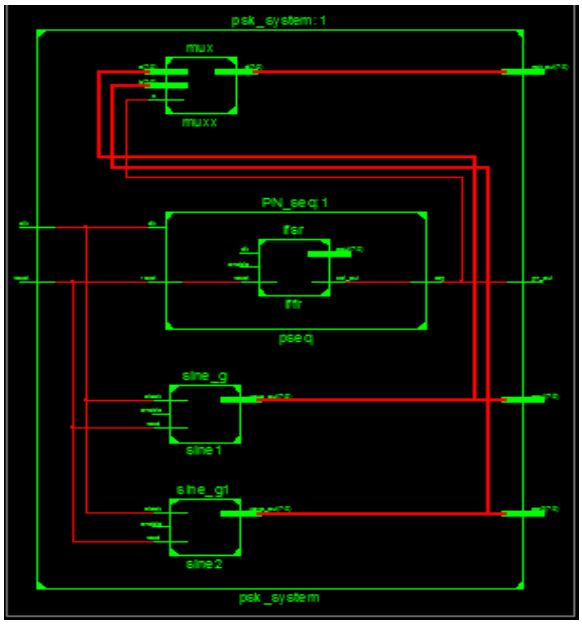

Fig 10 (e). RTL View of Modulator

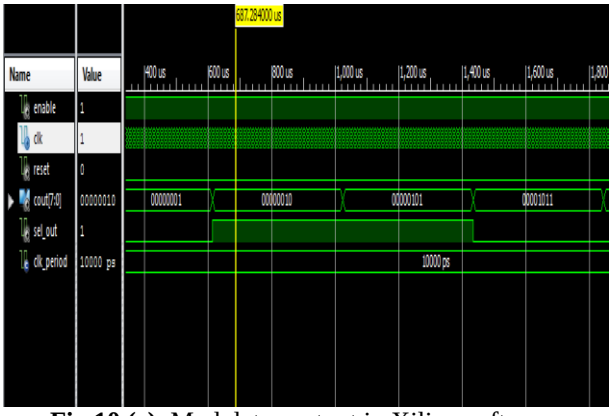

Fig 10 (e). Modulator output in Xilinx software

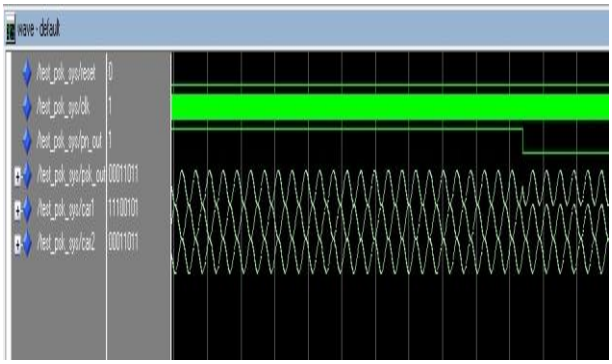

Fig 10 (g). Modulator output in modelsim software

2)Demodulator part:

Fig 11. Shows the complete demodulator block in which fisrt block is the sine wave generation block which is use to recover the strength of input signal,second block is the multiplier and third block is the accumulator.

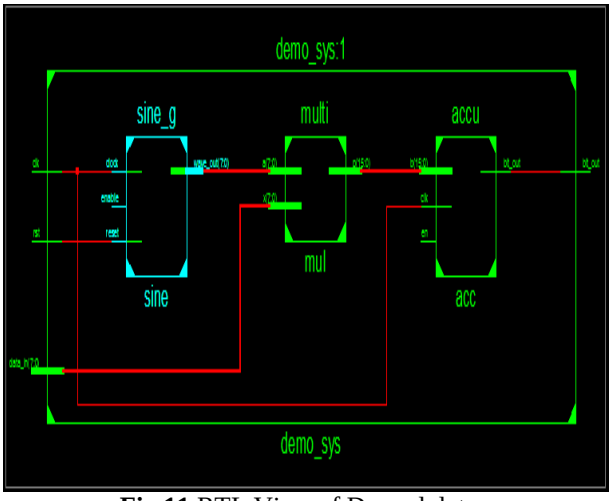

Fig 11.RTL View of Demodulator

3) Combine modulator and demodulator System:

Fig 12(a) represent the connection between modulator and demodulator.The output of modulator is given to the input of demodulator.Similarly fig 12(b) shows the internal blocks of modulator and demodulator.The final output of BPSK system is shown in fig 12(c) in which first signal is the input signal and second signal is the output of demodulator.

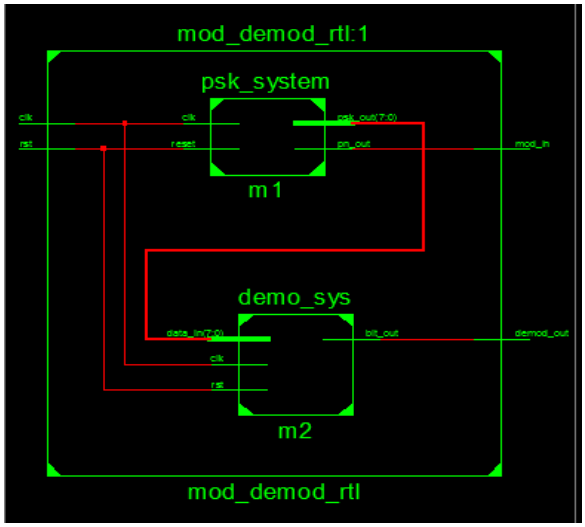

Fig 12 (a).RTL view of combine modulator and demodulator

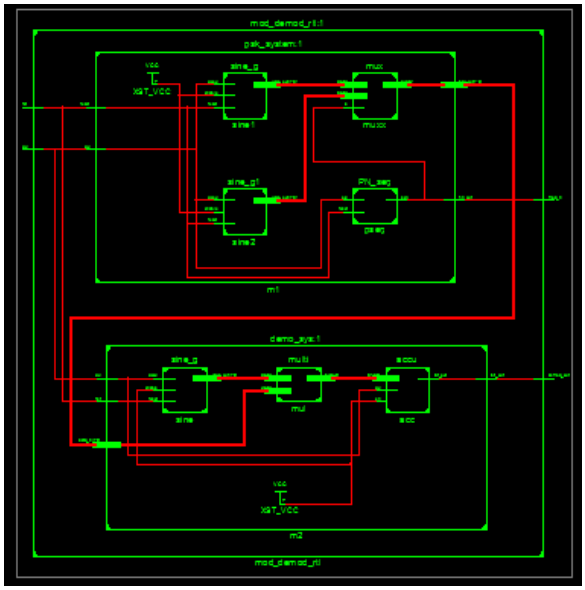

Fig 12(b). RTL View of modulator & demodulator system

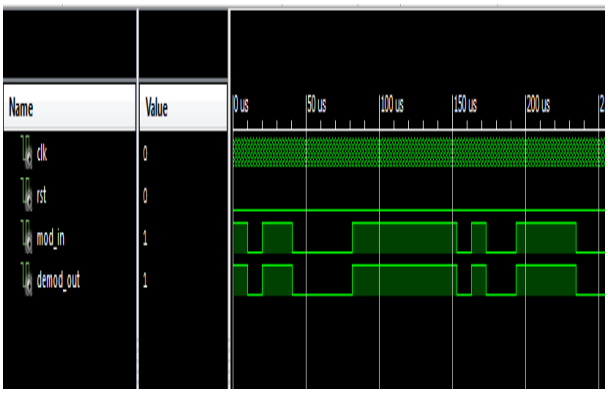

Fig 12 (c) Output waveform of modulator and demodulator

Fig.13 and 14 illustrate the design summary of modulator and demodulator board.The design summary shows the various synthesizer option that were enabled and some device utilization and timing statistics for the synthesized design.

Device Utilization Summary			
Logic Utilization	Used	Available	Utilization
Number of Slices:	111	768	14%
Number of Slice Flip Flops	29	1536	1%
Number of 4 input LUTs	208	1536	13%
Number used as logic	207		
Number used as Shift registers	1		
Number of IOs	27		
Number of bonded IOBs	27	124	21%
Number of GCLKs	1	8	12%

Fig 13. Design Summary of the BPSK Modulator

Device Utilization Summary			
Logic Utilization	Used	Available	Utilization
Number of Slices:	157	768	20%
Number of Slice Flip Flops	51	1536	3%
Number of 4 input LUTs	305	1536	19%
Number of IOs	11		
Number of bonded IOBs	11	124	8%
Number of GCLKs	1	8	12%

Fig 14. Design Summary of the BPSK Demodulator

VII. Conclusion

We represent the BPSK system (modulator and demodulator) using VHDL and implementation of the BPSK System on FPGA kit. The FPGA was selected as, compared to microcontrollers, it provides a larger number of input/output ports and the parallel implementation of hardware results in faster algorithm execution.

Both, the modulating signal and the carrier are generated internal, the modulating signal by a LFSR and the carrier by a DDS Compiler. The modulated signal is obtained at the output of a mux block and, then, passed through a communication channel where noise is added. In the demodulator, the carrier is recovered due to another DDS compiler and then multiplied with the modulated signal affected by noise. The obtained signal is then added with all the multiplied samples from the carrier in a period. The operation takes place in the accumulator. Once we have a result, it is compared with a decision threshold. If the compared signal is positive, the demodulator take the decision that '1' was transmitted, otherwise, '0'.

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